7I96
ETHERNET STEP/DIR MOTION CONTROL INTERFACE

V1.9

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GENERAL

DESCRIPTION

The 7I96 is a Ethernet connected motion control interface designed for interfacing up to 5 Axis of step and direction step motor or servo motor drives. Step rates up to 10 MHz are supported. The 7I96 also has 11 isolated inputs plus 6 isolated outputs for general purpose I/O use. A high speed encoder interface is provided for spindle synchronized motion. I/O expansion includes a RS-422/RS485 serial port and a parallel expansion port compatible with Mesa 25 pin daughtercards and standard parallel port breakouts.

All step and direction outputs are buffered 5V signals that can drive 24 mA. All outputs support differential mode to reduce susceptibility to noise. The spindle encoder can be used with TTL or differential input.

11 isolated inputs provided for general control use including limit switch and control panel inputs. Inputs operate with 4V to 36V DC and can have a positive or negative common for sourcing or sinking input applications. Six 36V 2A isolated outputs allow sinking, sourcing combinations of both.

One RS-422/RS-485 interface is provided for I/O expansion via a serial I/O daughtercard. In addition to the on card I/O, A FPGA expansion connector compatible with Mesa's 25 pin daughtercards or standard parallel port breakout boards allow almost unlimited I/O options including additional quadrature or absolute encoder inputs, step/dir or PWM/dir outputs, and field I/O expansion to hundreds of I/O of points. All field wiring is terminated in pluggable 3.5 mm screw terminal blocks.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I96 card is oriented in an upright position, that is, with the host interface RJ-45 connector pointing towards the left.

ENCODER INPUT MODE

The 7I96s high speed encoder input can be programmed for differential or single ended mode operation. W2, W3 and W4 set the encoder input mode. When W2,W3,and W4 are in the right hand position, the encoder input is mode is differential. When W2,W3, and W4 are in the left hand position, the encoder input mode is single ended or "TTL". Note that W4 controls the input mode for the ‘A’ signal, W3 controls the input mode for the ‘B’ signal and W2 controls the input mode for the index signal.

HARDWARE CONFIGURATION

EXPANSION CONNECTOR 5V POWER

The 7I96 has the option to supply 5V power to the breakout board connected to its expansion connector (P1).

The breakout 5V power is protected by a PTC device so will not cause damage to the 7I96 or cable if accidentally shorted. This option should only be enabled for Mesa breakout boards or boards specifically wired to accept 5V power on DB25 pins 22 through 25. When the option is disabled DB25 pins 22 through 25 are grounded. Jumper W8 controls the breakout power option.

JUMPER	POS	FUNCTION
W8	UP	5V BREAKOUT POWER ENABLED
W8	DOWN	5V BREAKOUT POWER DISABLED (*DEFAULT*)

EXPANSION CONNECTOR 5V I/O TOLERANCE

The FPGA used on the 7I96 has a 4V absolute maximum input voltage specification. To allow interfacing with 5V inputs on its expansion connector, the 7I96 has bus switches on all P1 expansion I/O pins. The bus switches work by turning off when the input voltage exceeds a preset threshold. *The 5V I/O tolerance option is the default and should normally be left enabled.*

For high speed applications where only 3.3V maximum signals are present, the 5V I/O tolerance option can be disabled. W7 controls the 5V I/O tolerance option. When W7 is on the default UP position, 5V tolerance mode is enabled. When W7 is in the DOWN position, 5V tolerance mode is disabled.

PULLUP VOLTAGE

In addition to selecting the input voltage tolerance mode, Jumper W7 also selects the pull-up resistor voltage, When W7 is in the UP position the 4.7K I/O pullup resistor common is connected to 5V, When W7 is in the down position, The 4.7K I/O pullup resistor common is connected to 3.3V.

JUMPER	POS	FUNCTION
W7	UP	5V I/O TOLERANCE / 5V PULLUPS (*DEFAULT*)
W7	DOWN	NO 5V TOLERANCE / 3.3V PULLUPS

HARDWARE CONFIGURATION

IP ADDRESS SELECTION

The 7I96 has three options for selecting its IP address. These options are selected by Jumpers W5 and W6.

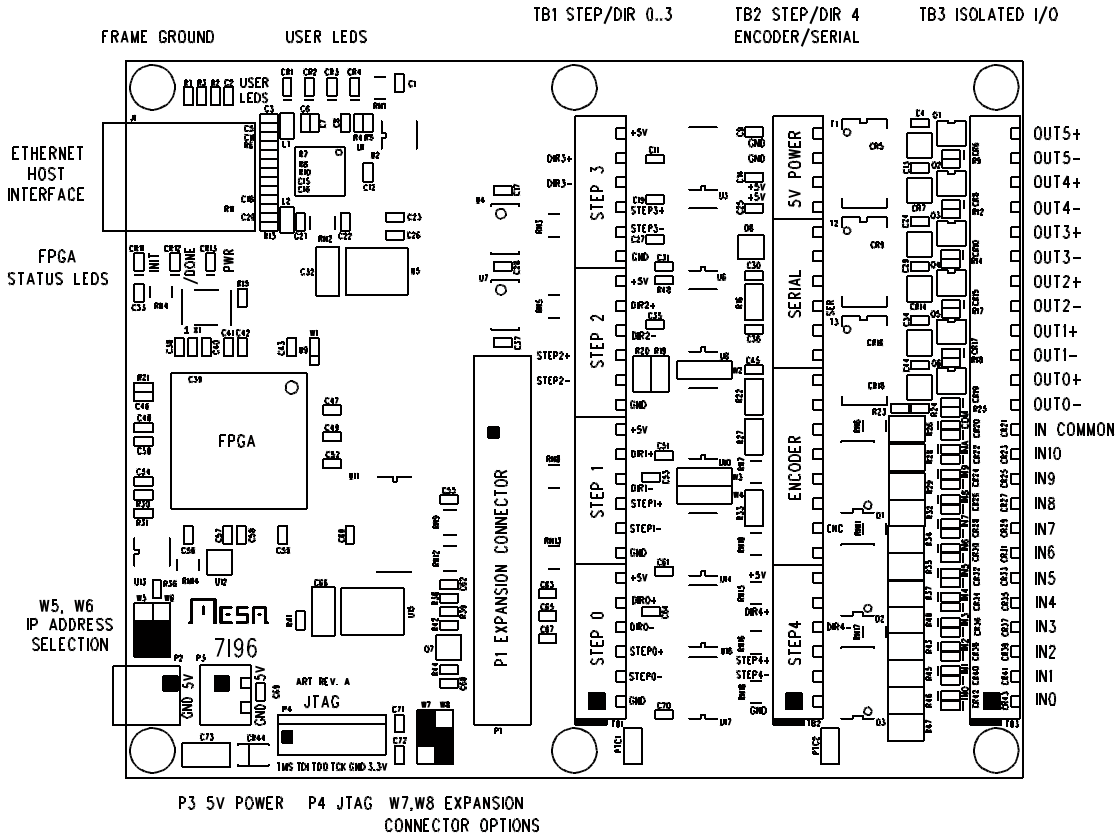
W5	W6	IP ADDRESS	
DOWN	DOWN	FIXED 192.168.1.121	(DEFAULT)
DOWN	UP	FIXED FROM EEPROM	
UP	DOWN	BOOTP	
UP	UP	INVALID	

Note: The as shipped default EEPROM IP address is 10.10.10.10. This can be changed via the mesaflash utility

CONNECTORS

7I96 CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS

NOTE: BLACK SQUARES INDICATE PIN 1



CONNECTORS

P3 POWER CONNECTOR PINOUT

P3 is the 7I96s 5V power connector. ***Do not supply any voltage other than 5V to P3!*** P3 is a 3.5MM plug-in screw terminal block. P3 pinout is as follows:

PIN	FUNCTION	
1	+5V	TOP, SQUARE PAD
2	GND	BOTTOM, ROUND PAD

P4 JTAG CONNECTOR PINOUT

P4 is a JTAG programming connector. This is normally used only for debugging or if both user and fallback EEPROM configurations have been corrupted. In case of corrupted EEPROM contents the EEPROM can be re-programmed using Xilinx's Impact tool.

P4 JTAG CONNECTOR PINOUT

PIN	FUNCTION
1	TMS
2	TDI
3	TDO
4	TCK
5	GND
6	+3.3V

FRAME GROUND

The top left mounting hole (near the Ethernet jack) is the frame ground connection. This should be grounded to earth/frame ground for best ESD/EMI resistance.

CONNECTORS

P1 EXPANSION CONNECTOR

The 7I96 has a 26 pin header to allow I/O expansion beyond the built in I/O on the 7I96 card. This I/O can include more step/dir channels, encoders, etc. This header has a pin-out that matches standard parallel port breakout cards and Mesa's 25 pin FPGA daughtercards, when terminated with a DB25 connector.

P1 PIN	DB25 PIN	P1 FUNC	P1 PIN	DB25 PIN	P1 FUNC
1	1	IO34	2	14	IO35
3	2	IO36	4	15	IO37
5	3	IO38	6	16	IO39
7	4	IO40	8	17	IO41
9	5	IO42	10	18	GND
11	6	IO43	12	19	GND
13	7	IO44	14	20	GND
15	8	IO45	16	21	GND
17	9	IO46	18	22	GND / 5V
19	10	IO47	20	23	GND / 5V
21	11	IO48	22	24	GND or 5V
23	12	IO49	24	25	GND or 5V
25	13	IO50	26	XX	GND or 5V

P1 header pins 18,20,22,24,26 (DB25 pins 22 through 25) can be tied to ground or 5V, depending on W8 position.

CONNECTORS

TB1 STEP AND DIR CONNECTOR

TB1 is the 7I96s main step and direction output connector. Both polarities of step and direction signals are provided. Each channel on the interface uses 6 pins. TB1 is a 3.5 MM pluggable terminal block with supplied removable screw terminal plugs.

TB1 CONNECTOR PINOUT

TB1 PIN	SIGNAL	TB1 PIN	SIGNAL
1	GND	13	GND
2	STEP0-	14	STEP2-
3	STEP0+	15	STEP2+
4	DIR0-	16	DIR2-
5	DIR0+	17	DIR2+
6	+5VP	18	+5VP
7	GND	19	GND
8	STEP1-	20	STEP3-
9	STEP1+	21	STEP3+
10	DIR1-	22	DIR3-
11	DIR1+	23	DIR3+
12	+5VP	24	+5VP

Note: 5VP pins are PTC short circuit protected 5V output pins for field wiring.

CONNECTORS

TB2 STEP/DIR, ENCODER RS-422 CONNECTOR

TB2 has a mix of signals including step/dir channel 4, an encoder interface, a RS-422/485 interface, and 5V logic supply power input. TB2 is a 24 terminal 3.5 MM pluggable terminal block with supplied removable screw terminal plugs.

TB2 CONNECTOR PINOUT

TB2 PIN	SIGNAL	TB2 PIN	SIGNAL
1	GND	13	IDX+
2	STEP4-	14	IDX-
3	STEP4+	15	GND
4	DIR4-	16	RS-422/485 RX+
5	DIR4+	17	RS-422/485 RX-
6	+5VP	18	RS-422 /485TX+
7	ENCA+	19	RS-422/485 TX-
8	ENCA-	20	+5VP
9	GND	21	5V IN
10	ENCB+	22	5V IN
11	ENCB-	23	GND
12	+5VP	24	GND

Note: 5VP pins are PTC short circuit protected 5V output pins for field wiring.

CONNECTORS

TB3 ISOLATED I/O CONNECTOR

Terminal block TB3 is the 7I96s isolated I/O connector. This has 11 4V-24V inputs and six isolated high current outputs.

TB3 CONNECTOR PINOUT

TB3 PIN	I/O	TB3 PIN	I/O
1	INPUT0	13	OUT0-
2	INPUT1	14	OUT0+
3	INPUT2	15	OUT1-
4	INPUT3	16	OUT1+
5	INPUT4	17	OUT2-
6	INPUT5	18	OUT2+
7	INPUT6	19	OUT3-
8	INPUT7	20	OUT3+
9	INPUT8	21	OUT4-
10	INPUT9	22	OUT4+
11	INPUT10	23	OUT5-
12	INPUT COMMON	24	OUT5+

OPERATION

RS-422/RS-485 INTERFACE

The 7I96 has one RS-422/RS-485 interface available on TB2. This interface is intended for I/O expansion with Mesa SSERIAL devices. The easiest way to make a cable for interfacing the 7I96 to these devices is to take a standard CAT5 or CAT6 cable, cut it in half, and wire the individual wires to the 7I96 screw terminals. The following chart gives the CAT5 to 7I96 screw terminal connections with EIA/TIA 568B colors:

TB2 PIN	SIGNAL	DIRECTION	CAT5 PIN	CAT5 568B COLOR
15	GND	FROM 7I96	4,5	BLUE, BLUE / WHITE
16	RX+	TO 7I96	6	GREEN
17	RX-	TO 7I96	3	GREEN / WHITE
18	TX+	FROM 7I96	2	ORANGE
19	TX-	FROM 7I96	1	ORANGE / WHITE
20	+5V	FROM 7I96	7,8	BROWN / WHITE,BROWN

Note: The 6 pin terminal block requires the +5V (brown and brown/white) and ground (blue and blue/white) pairs to be terminated in single screw terminal positions.

RS-485 OPERATION

For 2 wire RS-485 applications, TX+ must be connected to RX+ and TX- must be connected to RX-. **RS-485 pair wiring is TX-/RX- to A and TX+/RX+ to B**.

For RS-485 applications, 7I96 cards require two biasing resistors to establish the non-driven state of RS-485 interfaces (MODBUS etc). The first resistor should connect between +5V and RX- and the second between GND and RX+. Suggested resistor value is 330 Ohms.

OPERATION

STEP/DIR INTERFACE

The 7I96 provides five channels of step/dir interface with buffered 5V differential signal pairs. Each differential pair consists of two complementary 5V outputs. The differential signals allows reliable signal transmission in noisy environments and can directly interface with RS-422 line receivers. Step motor drives with single ended inputs connect to just one of the STEP and DIR signal outputs, that is either the STEP+/DIR+ or STEP-/DIR- signals, with the unused signals left unconnected at the 7I96. The input common signal on drives with single ended inputs connects to the 7I96s GND or 5VP pins depending on the drive type.

ENCODER INTERFACE

The 7I96 provides a one channel encoder interface with index. This is intended as a spindle encoder but can be used for other purposes. The encoder input can be programmed for differential or single ended encoders. The encoder interface also provides short circuit protected 5V power to the encoder. When used with single ended encoders, the ENCA+, ENCB+ and IDX+ signals are wired to the encoder and the ENCA-,ENCB-, and IDX- terminals are left unconnected.

OPERATION

BOARD STATUS LEDS

The 7I96 has seven LEDS for card status monitoring. The color, function and locations are as follows:

LED	COLOR	FUNCTION	OK	LOCATION
CR11	YELLOW	FPGA /INIT	OFF	TOP LEFT
CR12	RED	FPGA /DONE	OFF	TOP LEFT
CR13	YELLOW	LOGIC POWER	ON	TOP LEFT
CR1	GREEN	USER LED3	ANY	TOP LEFT
CR2	GREEN	USER LED2	ANY	TOP LEFT
CR3	GREEN	USER LED1	ANY	TOP LEFT
CR4	GREEN	USER LED0	ANY	TOP LEFT

In normal operation CR11 and CR12 will be off. If either is on after power-up there is a problem with configuring the FPGA. CR11 is also used to signal a HostMot2 watchdog bite so will be illuminated when the LinuxCNC exits. CR13 (power LED) will also be on. The user LEDs default function counts received packets but their function can be changed to user accessible HostMot2 LEDs if desired.

I/O STATUS LEDS

In addition to the board status LEDs, each isolated input and output has an associated yellow LED that illuminates when the input or output is active.

OPERATION

ISOLATED I/O

The 7I96 has 11 isolated inputs and 6 isolated outputs. All 11 Isolated inputs have a common pin. This common pin must be connected to ground for active high inputs (PNP type) and connected to the I/O power for active low inputs (NPN type). The 6 isolated outputs are completely floating switches so can be use for pull-up/pull-down and mixed voltage switching.

ISOLATED INPUT CHARACTERISTICS

The isolated inputs use opto-isolators with a 4.7K input series resistance. This results in an approximate current draw of 5 mA at 24V. The inputs will operate with +-4V to +-36V signals relative to input common. Isolated inputs are relatively slow and not suited for signals faster than about 5 KHz.

For PNP type sensors or switches with a common positive, the input common pin is grounded and the sensor or switch applies a positive voltage to the input pin to activate the input.

For NPN type sensors or switches with a common ground, the input common is connected to +5 to +36V and the input pins are grounded to activate an input.

ISOLATED OUTPUT CHARACTERISTICS

The 6 isolated outputs use full floating MOSFET switches (a DC Solid State Relay or SSR) and can be used just like a switch or relay contact. Maximum voltage is 36 VDC and maximum load current is 2A. Inductive loads must have a flyback diode. The output polarity must be observed (reversed outputs will be stuck-on).

Note: The 7I96 outputs are not short circuit protected so a current limited power supply or a 2A to 5A fuse should be used in the power source that supplies the outputs.

HOST INTERFACE

FPGA

The 7I96 use a Xilinx Spartan6 FPGA in a TQFP 144 package: XC6SLX9-2TQG144.

IP ADDRESS SELECTION

Initial communication with the 7I96 requires knowing its IP address. The 7I96 has 3 IP address options: Default, EEPROM, and Bootp, selected by jumpers W5 and W6. Default IP address is always 192.168.1.121. The EEPROM IP address is set by writing Ethernet EEPROM locations 0x20 and 0X22. BootP allows the 7I96 address to be set by a DHCP/ BootP server. If BootP is chosen, the 7I96 will retry BootP requests at a ~1 Hz rate if the BootP server does not respond.

HOST COMMUNICATION

The 7I96 standard firmware is designed for low overhead real time communication with a host controller so implements a very simple set of IPV4 operations. These operations include ARP reply, ICMP echo reply, and UDP packet receive/send for host data communications. UDP is used so that the 7I96 can be used on a standard network with standard tools for non-real time applications. No fragmentation is allowed so maximum packet size is 1500 bytes.

UDP

All 7I96 Ethernet communication is done via UDP packets. The 7I96 socket number for UDP data communication is 27181. Read data is routed to the requesters port number. Under UDP, a simple register access protocol is used. This protocol is called LBP16.

LBP16

LBP16 allows read and write access to up to eight separate address spaces with different sizes and characteristics. Current firmware uses seven of these spaces. For efficiency, LBP16 allows access to blocks of registers at sequential increasing addresses. (Block transfers)

WINDOWS ARP ISSUES

The Windows XP and earlier TCP stack has a characteristic that causes it to drop outgoing UDP packets when refreshing its ARP cache. Because of this you must either verify packet transmission via echoing data from the 7I96 for every transaction (reading RXUDPCount is suggested) and retrying failed transactions, or alternatively, setting up a static entry for the 7I96 in the ARP table. This is done with windows ARP command.

HOST INTERFACE

CONFIGURATION

The 7I96 is configured at power up by a SPI FLASH memory. This flash memory is an 16M bit chip that has space for two configuration files. Since all Ethernet logic on the 7I96 is in the FPGA, a problem with configuration means that Ethernet access will not be possible. For this reason there is a backup method to recover from FPGA boot failures.

FALLBACK

The backup system is called Fallback. The 7I96 flash memory normally contains two configuration file images, A user image and a fallback image. If the primary user configuration is corrupted, the FPGA will load the fallback configuration so the flash memory image can be repaired remotely without having to resort JTAG programming.

Note that if you program the 7I96 with a valid bitfile for a XC6SLX9 but not designed for a 7I96, you will likely "brick" the card. The only way a bricked card can be recovered is by using JTAG.

HOST INTERFACE

EEPROM LAYOUT

The EEPROM used on the 7I96 for configuration storage is the M25P16. The M25P16 is a 16 M bit (2 M byte) EEPROM with 32 64K byte sectors. Configuration files are stored on sector boundaries to allow individual configuration file erasing and updating. Standard EEPROM sector layout is as follows:

0x000000	BOOT BLOCK
0x010000	FALLBACK CONFIGURATION BLOCK 0
0x020000	FALLBACK CONFIGURATION BLOCK 1
0x030000	FALLBACK CONFIGURATION BLOCK 2
0x040000	FALLBACK CONFIGURATION BLOCK 3
0x050000	FALLBACK CONFIGURATION BLOCK 4
0x060000	FALLBACK CONFIGURATION BLOCK 5
0x070000	UNUSED/FREE
0x080000	UNUSED/FREE
0x090000	UNUSED/FREE
0x0A0000	UNUSED/FREE
0x0B0000	UNUSED/FREE
0x0C0000	UNUSED/FREE
0x0D0000	UNUSED/FREE
0x0E0000	UNUSED/FREE
0x0F0000	UNUSED/FREE

HOST INTERFACE

EEPROM LAYOUT

0x100000	USER CONFIGURATION BLOCK 0
0x110000	USER CONFIGURATION BLOCK 1
0x120000	USER CONFIGURATION BLOCK 2
0x130000	USER CONFIGURATION BLOCK 3
0x140000	USER CONFIGURATION BLOCK 4
0x150000	USER CONFIGURATION BLOCK 5
0x160000	UNUSED/FREE
0x170000	UNUSED/FREE
0x180000	UNUSED/FREE
0x190000	UNUSED/FREE
0x1A0000	UNUSED/FREE
0x1B0000	UNUSED/FREE
0x1C0000	UNUSED/FREE
0x1D0000	UNUSED/FREE
0x1E0000	UNUSED/FREE
0x1F0000	UNUSED/FREE

HOST INTERFACE

BITFILE FORMAT

The configuration utilities expect standard FPGA bitfiles without any multiboot features enabled. If multiboot FPGA files are loaded they will likely cause a configuration failure. In addition for fallback to work, the -g next_config_register_write:disable, -g reset_on_error:enable and -g CRC:enable bitgen options must be set.

MESAFLASH

Linux and Windows utility programs MESAFLASH are provided to write configuration files to the 7I96 EEPROM. These files depend on a simple SPI interface built into both the standard user FPGA bitfiles and the fallback bitfile. *The MESAFLASH utilities expect standard FPGA bitfiles without any multiboot features enabled. If multiboot FPGA files are loaded they will likely cause a configuration failure.*

If mesaflash is run with a –help command line argument it will print usage information.

The following examples assume the target 7I96 is using the ROM IP address of 192.168.1.121.

```
mesaflash --device 7I96 --write FPGAFILE.BIT
```

Writes a standard bitfile FPGAFILE.BIT to the user area of the EEPROM.

```
mesaflash --device 7I96 --verify FPGAFILE.BIT
```

Verifies the user EEPROM configuration against the bit file FPGAFILE.BIT.

```
mesaflash --device 7I96 --fallback --write FALLBACK.BIT
```

Writes the fallback EEPROM configuration to the fallback area of the EEPROM. In addition if the bootblock is not present in block 0 of the EEPROM, it re-writes the bootblock.

SETTING EEPROM IP ADDRESS

MESAFLASH can also write the EEPROM IP address of the 7I96:

```
MESAFLASH --device 7I96 --set ip=192.168.0.100
```

The above examples assume the 7I96 has its default ROM IP address (192.168.1.121). If the 7I96 is using another IP address, this must be specified on the command line with a –addr XX.XX.XX.XX command line argument.

HOST INTERFACE

FREE FLASH MEMORY SPACE

Ninteen 64K byte blocks of flash memory space are free when both user and fallback configurations are installed on the 7I96. It is suggested that only the last two blocks, 0x1E0000 and 0x1F0000 in the user area, be used for FPGA application flash storage.

FALLBACK INDICATION

Mesa's supplied fallback configurations blink the red INIT LED on the top right hand side of the card if the primary configuration fails and the fallback configuration loaded successfully. If this happens it means the user configuration is corrupted or not a proper configuration for the 7I96s FPGA. This can be fixed by running the configuration utility and re-writing the user configuration**.**

FAILURE TO CONFIGURE

The 7I96 should configure its FPGA within a fraction of a second of power application. If the FPGA card fails to configure, the red /DONE LED CR2 will remain illuminated. If this happens, the 7I96s EEPROMs must be re-programmed via the JTAG connector or (faster) JTAG FPGA load followed by Ethernet EEPROM update.

CLOCK SIGNALS

The 7I96 has a single 50 MHz clock signal from an on card crystal oscillator. The clock a can be multiplied and divided by the FPGAs clock generator block to generate a wide range of internal clock signals. The 50 MHz clock is also used to generate the 25MHz clock for the Ethernet interface chip.

HOST INTERFACE

LOGIC POWER

5V logic power for the host interface FPGA, expansion connectors, RS-422 and encoder connections and step/dir connections can be provided at connector P3, or alternatively TB2.

PULLUP RESISTORS

All expansion I/O pins are provided with pull-up resistors to allow connection to open drain, open collector, or OPTO devices. These resistors have a value of 4.7K so have a maximum pull-up current of ~1.07 mA (5V pull-up) or ~.7 mA (3.3V pull-up).

EXPANSION CONNECTOR IO LEVELS

The Xilinx FPGAs used on the 7I96 have programmable I/O levels for interfacing with different logic families. The 7I96 does not support use of the I/O standards that require input reference voltages. All standard Mesa configurations use LVTTL levels.

Note that even though the 7I96 expansion I/O can tolerate 5V signal inputs, its outputs will not swing to 5V. The outputs are push pull CMOS that will drive to the output supply rail of 3.3V. This is sufficient for TTL compatibility but may cause problems with some types of loads. For example when driving an LED that has its anode connected to 5V, in such devices as OPTO isolators and I/O module rack SSRs, the 3.3V high level may not completely turn the LED off. To avoid this problem, either drive loads that are ground referred, Use 3.3V as the VCC for VCC referred loads, or use open drain mode.

EXPANSION CONNECTOR STARTUP I/O VOLTAGE

After power-up or system reset and before the the FPGA is configured, the pull-up resistors will pull all I/O signals to a high level. If the FPGA is used for motion control or controlling devices that could present a hazard when enabled, external circuitry should be designed so that this initial state (high) results in a safe condition.

REFERENCE INFORMATION

LBP16

GENERAL

LBP16 is the simple register access protocol used by the 7I96 for all Ethernet communications.

LBP16 COMMANDS

LBP16 is a simple remote register access protocol to allow efficient register access over the Ethernet link. All LBP16 commands are 16 bits in length and have the following structure:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	A	C	M	M	M	S	S	I	N	N	N	N	N	N	N

W Is the write bit (1 means write, 0 means read)

A Is the includes Address bit. If this is '1' the command is followed by a 16 bit address and the address pointer is loaded with this address. if this is 0 the current address pointer for the memory space is used. Each memory space has its own address pointer.

C Indicates if memory space itself (C=’0') or associated info area for the memory will be accessed (C= ‘1')

M Is the 3 bit memory space specifier 000b through 111b

S Is the transfer element size specifier (00b = 8 bits, 01b = 16 bits 10b = 32 bits and 11b = 64 bits)

I Is the Increment address bit. if this is '1' the address pointer is incremented by the element transfer size (in bytes) after every transfer ('0' is useful for FIFO transfers)

N Is the transfer count in units of the selected size. 1 through 127. A transfer count of 0 is an error.

LBP16 read commands are followed by the 16 bit address (if the A bit is set). LBP16 Write commands are followed by the address (if bit A is set) and the data to be written. LBP16 Addresses are always byte addresses. LBP data and addresses are little endian so must be sent LSB first.

REFERENCE INFORMATION

LBP16

INFO AREA

There are eight possible memory spaces in LBP16. Each memory space has an associated read only info area. The first entry has a cookie to verify correct access. The next two entries in the info area are the MemSizes word and the MemRanges word. Only 16 bit read access is allowed to the info area.

0000	COOKIE = 0X5A0N WHERE N = ADDRESS SPACE 0..7
0002	MEMSIZES
0004	MEMRANGES
0006	ADDRESS POINTER
0008	SPACENAME 0,1
000A	SPACENAME 2,3
000C	SPACENAME 4,5
000E	SPACENAME 6,7

INFO AREA MEMSIZES FORMAT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	T	T	T	T	T	T	T	X	X	X	X	A	A	A	A

W Memory space is Writeable

T Is type: 01 = Register, 02 = Memory, 0E = EEPROM, 0F = Flash

A Is access types (bit 0 = 8 bit, bit 1 = 16 bit etc)so for example 0x06 means 16 bit and 32 bit operations allowed

REFERENCE INFORMATION

LBP16

INFO AREA MEMRANGES FORMAT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E	E	E	E	E	P	P	P	P	P	S	S	S	S	S	S

E Is erase block size

P Is Page size

S Ps address range

Ranges are 2^E, 2^P, 2^S. All sizes and ranges are in bytes. E and P are 0 for non-flash memory

REFERENCE INFORMATION

LBP16

INFO_AREA ACCESS

As discussed above, all memory spaces have an associated information area that describes the memory space. Information area data is all 16 bits and read-only.The hex command examples below are written in LSB first order for convenience. In the hex command examples, the NN is the count/increment field of the LBP16 command and the LLHH is the low and high bytes of the address.

Ispace 0 read with address	NN61LLHH	HostMot2 space
Ispace 0 read	NN21	
Ispace 1 read with address	NN65LLHH	Ethernet chip space
Ispace 1 read	NN25	
Ispace 2 read with address	NN69LLHH	Ethernet EEPROM space
Ispace 2 read	NN29	
Ispace 3 read with address	NN6DLLHH	FPGA flash space
Ispace 3 read	NN2D	
Ispace 6 read with address	NN79LLHH	LBP16 R/W space
Ispace 6 read	NN39	
Ispace 7 read with address	NN7DLLHH	LBP16 R/O space
Ispace 7 read	NN3D	

REFERENCE INFORMATION

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7I96 SUPPORTED MEMORY SPACES

The 7I96 firmware supports 6 address spaces. These will be described individually with example hexadecimal commands. The hex command examples below are written in LSB first order for convenience. In the hex command examples, the NN is the count/increment field of the LBP16 command and the LLHH is the low and high bytes of the address.

SPACE 0: HOSTMOT2 REGISTERS

This address space is the most important as it gives access to the FPGA I/O. This is a 64K byte address range space with 32 bit R/W access.

Space 0 read with address	NN42LLHH
Space 0 write with address	NNC2LLHH
Space 0 read	NN02
Space 0 write	NN82

REFERENCE INFORMATION

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SPACE 0: HOSTMOT2 REGISTERS

Example: read first 5 entries in hostmot2 IDROM:

85420004

85	; 85 == NN = 5 | Inc bit (0x80) so address is incremented after each access
42	; Read from space 0 with address included after command
00	; LSB of address (IDROM starts at 0x0400)
04	; MSB of address (IDROM starts at 0x0400)

Example: write 4 GPIO ports starting at 0x1000:

84C20010AAAAAAAABBBBBBBBCCCCCCCCDDDDDDDD

84	; 84 == NN = 4 | Inc bit so address is incremented after each access
C2	; Write to space 0 with address included after command
00	; LSB of address (GPIO starts at 0x1000)
10	; MSB of address (GPIO starts at 0x1000)
AAAAAAAA	; 32 bit data for GPIO port 0 at 0x1000
BBBBBBBB	; 32 bit data for GPIO port 0 at 0x1004
CCCCCCCC	; 32 bit data for GPIO port 0 at 0x1008
DDDDDDDD	; 32 bit data for GPIO port 0 at 0x100C

Note like all LBP16 data, write data is LS byte first

REFERENCE INFORMATION

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SPACE 1: ETHERNET CHIP ACCESS

Space 1 allows access to the KSZ8851-16 registers for debug purposes. All accesses are 16 bit.

Space 1 read with address	NN45LLHH
Space 1 write with address	NNC5LLHH
Space 1 read	NN05
Space 1 write	NN85

Example: read Ethernet chip CIDER register: 0145C000

01	; = NN = read 1 16 bit value
45	; read space 1 with address included
C0	; LSB of CIDER address
00	; MSB of CIDER address

SPACE 2: ETHERNET EEPROM CHIP ACCESS

This space is used to store the Ethernet MAC address, card name, and EEPROM settable IP address. The Ethernet EEPROM space is accessed as 16 bit data. The first 0x20 bytes are read only and the remaining 0x60 bytes are read/write.

Space 2 read with address	NN49LLHH
Space 2 write with address	NNC9LLHH
Space 2 read	NN09
Space 2 write	NN89

REFERENCE INFORMATION

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SPACE2: ETHERNET EEPROM CHIP ACCESS

Writes and erases require that the EEPROMWEna be set to 5A02. *Note that EEPROMWEna is cleared at the end of every LPB packet so the write EEPROMWEna command needs to prepended to all EEPROM write and erase packets.* For EEPROM write operations a LBP16 read operation should follow the write(s) for host synchronization.

Example: write EEPROM IP address with 192:168.0.32 (C0:A8:0:20 in hex)

01D91A00025A	Enable EEPROM area writes
82C920002000A8C0	Write 2 words to 0020 : C0A80020 (with inc). Note this must be in the same packet and the EEPROMWEna write

ETHERNET EEPROM LAYOUT

ADDRESS	DATA
0000	Reserved RO
0002	MAC address LS Word RO
0004	MAC address Mid Word RO
0006	MAC address MS Word RO
0008	Reserved RO
000A	Reserved RO
000C	Reserved RO
000E	Unused RO

REFERENCE INFORMATION

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ETHERNET EEPROM LAYOUT

ADDRESS	DATA
0010	CardNameChar-0,1 RO
0012	CardNameChar-2,3 RO
0014	CardNameChar-4,5 RO
0016	CardNameChar-6,7 RO
0018	CardNameChar-8,9 RO
001A	CardNameChar-10,11 RO
001C	CardNameChar-12,13 RO
001E	CardNameChar-14,15 RO
0020	EEPROM IP address LS word RW
0022	EEPROM IP address MS word RW
0024	EEPROM Netmask LS word RW (V16 and > firmware)
0026	EEPROM Netmask MS word RW (V16 and > firmware)
0028	DEBUG LED Mode (LS bit determines HostMot2 (0) or debug(1)) RW
002A	Reserved RW
002C	Reserved RW
002E	Reserved RW
0030..007E	Unused RW

REFERENCE INFORMATION

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SPACE 3: FPGA FLASH EEPROM CHIP ACCESS

Space 3 allows access to the FPGAs configuration flash memory. All flash memory access is 32 bit. Flash memory access is different from other memory spaces in that it is done indirectly via a 32 bit address pointer and 32 bit data port.

Space 3 read with address NN4ELLHH

Space 3 write with address NNCELLHHDDDDDDDD

Space 3 read NN0E

Space 3 write NN8E

FLASH MEMORY REGISTERS

Flash memory spaces have only 4 accessible registers:

ADDRESS	DATA	
0000	FL_ADDR	32 bit flash address register
0004	FL_DATA	32 bit flash data register
0008	FL_ID	32 bit read only flash ID register
000C	SEC_ERASE	32 bit write only sector erase register

Unlike other memory spaces, flash memory space is accessed indirectly by writing the address register (FL_ADDR) and then reading or writing the data (FL_DATA). The flash byte address is automatically incremented by 4 each data access.

Note that reads can read all of flash memory with consecutive read operations but write operations can only write a flash page worth of data before the page write must be started. Also unless you are doing partial page writes, page write should always start on a page boundary.

The page write is started by writing the flash address, reading the flash address, reading flash data, reading flash ID or issuing a erase sector command. For host synchronization, a read operation should follow every sector erase or page write.

REFERENCE INFORMATION

LBP16

SPACE 3: FPGA FLASH EEPROM CHIP ACCESS

Example: read 1024 bytes (0100h doublewords) of flash space at address 00123456:

01CE000056341200	Write FL_ADDR (0000) with pointer (0x00123456)
404E0400	Issue read command (FL_DATA = 0004) With count of 0x40 double words (256 bytes). Note do not use LBP16 increment bit! Flash address always autoincremented
400E	Next 0x40 doublewords = 256 bytes
400E	Next 0x40 doublewords = 256 bytes
400E	Next 0x40 doublewords = 256 bytes

Note that this is close to the maximum reads allowed in a single LBP packet (~1450 bytes)

Writes and erases require that the EEPROMWEna be set to 5A03. *Note that EEPROMWEna is cleared at the end of every LPB packet so the write EEPROMWEna command needs to prepended to all flash write and erase packets. The following is written on separate lines for clarity but must all be in one packet for correct operation.*

Example: Write a 256 byte page of flash memory starting at 0xC000:

01D91A00035A	Write EEPROMWEna with 0x5A03
01CE000000C00000	Write flash address
40CE0400	Issue write flash data command with count
12345678	Doubleword 0
ABCD8888	Doubleword 1
...	
FFFFFFFF	Doubleword 63 (= 256 bytes)
014E0000	Read new address to commit write and so some data is returned for host synchronization (so host waits for write to complete)

REFERENCE INFORMATION

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SPACE 3: FPGA FLASH EEPROM CHIP ACCESS

Example: Erase flash sector 0x00010000:

01D91A00035A	Write EEPROMWEna with 0x5A03
01CE000000000100	Write flash address with 0x 00010000
01CE0C0000000000	Write sector erase command (with dummy 32 bit data = 0)
014E0000	Read flash address for host synchronization (this will echo the address _after_ the sector is erased)

REFERENCE INFORMATION

LBP16

SPACE 4 LBP TIMER/UTILITY AREA

Address space 4 is for read/write access to LBP specific timing registers. All memory space 4 access is 16 bit.

Space 4 read with address	NN51LLHH
Space 4 write with address	NND1LLHHDDDD
Space 4 read	NN11
Space 4 write	NN91DDDD

MEMORY SPACE 4 LAYOUT:

ADDRESS	DATA
0000	uSTimeStampReg
0002	WaituSReg
0004	HM2Timeout
0006	WaitForHM2RefTime
0008	WaitForHM2Timer1
000A	WaitForHM2Timer2
000C	WaitForHM2Timer3
000E	WaitForHM2Timer4
0010..001E	Scratch registers for any use

The uSTimeStamp register reads the free running hardware microsecond timer. It is useful for timing internal 7I96 operations. Writes to the uSTimeStamp register are a no-op. The WaituS register delays processing for the specified number of microseconds when written, (0 to 65535 uS) reads return the last wait time written. The HM2TimeOut register sets the timeout value for all WaitForHM2 times (0 to 65536 uS).

All the WaitForHM2Timer registers wait for the rising edge of the specified timer or reference output when read or written, write data is don't care, and reads return the wait time in uS. The HM2TimeOut register places an upper bound on how long the WaitForHM2 operations will wait. HM2Timeouts set the HM2TImeout error bit in the error register.

REFERENCE INFORMATION

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SPACE 6 LBP STATUS/CONTROL AREA

Address space 6 is for read/write access to LBP specific control, status, and error registers. All memory space 6 access is 16 bit. The RXUDPCount and TXUDPCount can be used as sequence numbers to verify packet reception and transmission.

Space 6 read with address	NN59LLHH
Space 6 write with address	NND9LLHHDDDD
Space 6 read	NN19
Space 6 write	NN99DDDD

MEMORY SPACE 6 LAYOUT:

ADDRESS	DATA
0000	ErrorReg
0002	LBPParseErrors
0004	LBPMemErrors
0006	LBPWriteErrors
0008	RXPktCount
000A	RXUDPCount
000C	RXBadCount
000E	TXPktCount
00010	TXUDPCount
00012	TXBadCount

REFERENCE INFORMATION

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MEMORY SPACE 6 LAYOUT:

ADDRESS	DATA	
0014	LEDMode	If LSb is 0, LEDs are "owned" by HostMot2, otherwise LEDs are local debug LEDs
0016	DebugLEDPtr	What variable in space 6 local debug LEDs show (default is RXPktCount).
0018	Scratch	Can be used for sequence numbers
001A	EEPROMWEna	Must be set to 5A0N to enable EEPROM or flash writes or erases (N is memory space of EEPROM or flash) Note that this is cleared at the end of every packet.
001C	LBPReset	Setting this to a non-zero value will do a full reset of the LBP16 firmware. The 7I96 will read ita IP address jumpers and re-assign its IP address. The 7I96 will be unresponsive for as much as ½ of a second after this command.
001E	FPGAICAP	FPGA ICAP-16 register to allow remote FPGA reload and other low level FPGA access.

ERROR REGISTER FORMAT

BIT	ERROR
0	LBPParseError
1	LBPMemError
2	LBPWriteError
3	RXPacketErr
4	TXPacketErr
5	HM2TimeOutError
6..15	Reserved

REFERENCE INFORMATION

LBP16

SPACE 7: LBP READ ONLY AREA

Memory space 7 is used for read only card information. Memory space 7 is accessed as 16 bit data.

Space 7 read with address	NN5DLLHH
Space 7 read	NN1D

MEMORY SPACE 7 LAYOUT:

ADDRESS	DATA	
0000	CardNameChar-0,1	
0002	CardNameChar-2,3	
0004	CardNameChar-4,5	
0006	CardNameChar-6,7	
0008	CardNameChar-8,9	
000A	CardNameChar-10,11	
000C	CardNameChar-12.13	
000E	CardNameChar-14,15	
0010	LBPVersion	
0012	FirmwareVersion	
0014	Option Jumpers	
0016	Reserved	
0018	RecvStartTS	1 uSec timestamps
001A	RecvDoneTS	For performance monitoring
001C	SendStartTS	Send timestamps are
001E	SendDoneTS	from ***previous*** packet

REFERENCE INFORMATION

LBP16

ELBPCOM

ELBPCOM is a very simple demo program in Python (2.x) to allow simple checking of LBP16 host communication to the 7I96. ELBPCOM accepts hexadecimal LBP16 commands and data and returns hexadecimal results. Note that the timeout value will need to be increased to about 2 seconds to try flash sector erase commands.

```
import socket
s = socket.socket(socket.AF_INET,socket.SOCK_DGRAM,0)
sip  = "192.168.1.121"
sport = 27181
s.settimeout(.2)
while(2 >0):
 sdata = raw_input ('>')
 sdata = sdata.decode('hex')
 s.sendto(sdata,(sip,sport))
 try:
  data,addr = s.recvfrom(1280)
  print ('>'),data.encode('hex')
 except socket.timeout:
  print ('No answer')
```

Sample run:

```
>01420001                       ; read hostmot2 cookie at 0x100
> fecaaa55                      ; 7I96 returns 0x55AACAFE

>82492000                       ; read EEPROM IP address at 0x0020
> 450a5863                      ; 63:58:0A:45 = 99.88.10.69
                                ;(for example)

>01D91A00025A82C920000100a8C0 ; write EEPROM IP address
                                ;(at 0x0020) with
                                ; C0:A8:0:1 = 192.168.0.1
```

REFERENCE INFORMATION

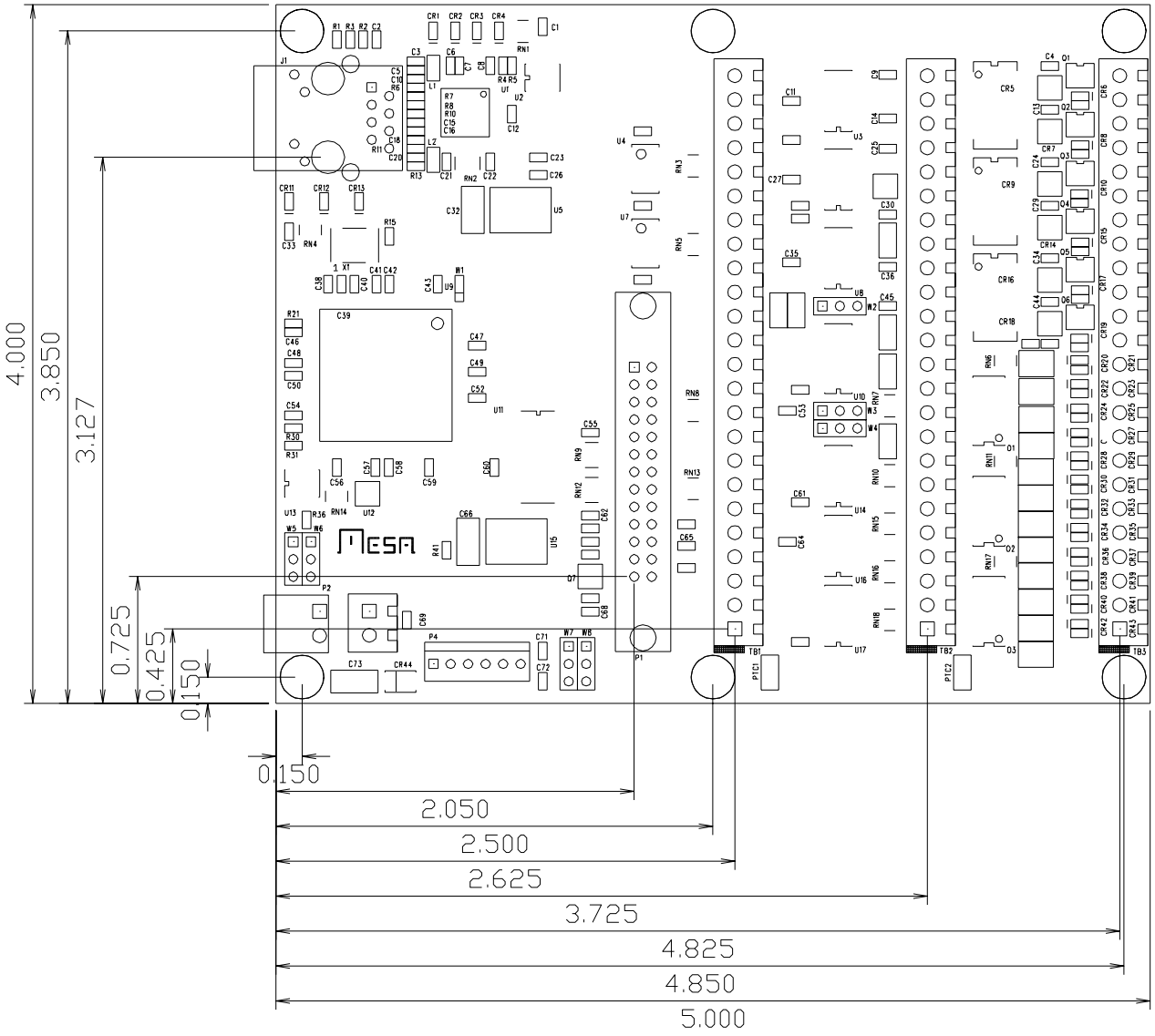
SPECIFICATIONS

	MIN	MAX	NOTES
GENERAL			
HOST SUPPLY VOLTAGE 5V	4.75 VDC	5.25 VDC	
5V CURRENT	----	250 mA	No ext load .
STEP/DIR OUTPUTS			
STEP/DIR OUTPUT HIGH V	4V	----	10 mA source
STEP/DIR OUTPUT LOW V	----	1V	10mA sink
STEP RATE	----	10	MHz
ISOLATED INPUTS			
INPUT RANGE	+-4V	+-36V	
INPUT RESISTANCE	4.7K	5K	
INPUT ISOLATION VOLTAGE	----	100	VDC
MAXIMUM INPUT FREQUENCY	----	5	KHz
ISOLATED OUTPUTS			
OUTPUT SWITCHED VOLTAGE	0V	+36V	
OUTPUT SWITCHED CURRENT	----	2A	
OUTPUT RESISTANCE	----	75	mOhm
OUTPUT ISOLATION VOLTAGE	----	100	VDC
MAXIMUM OUTPUT FREQUENCY	----	5	KHz

REFERENCE INFORMATION

SPECIFICATIONS

		MIN	MAX	NOTES
HIGH SPEED ENCODER INPUT				
INPUT COMMON MODE RANGE		-7	+12	Volts
INPUT TTL MODE THRESHOLD		1.4	1.8	Volts
DIFFERENTIAL MODE IMPEDANCE		118	122	Ohms
COUNT RATE		----	10 MHz	
RS-422/RS485 INTERFACE				
MAXIMUM DATA RATE		----	5	MBIT/S
INPUT COMMON MODE RANGE		-7	+12	Volts
INPUT TERMINATION RESISTOR		118	122	Ohm
OUTPUT LOW	(24 mA sink)	----	.8	Volts
OUTPUT HIGH	(24 mA source)	VCC-2	----	Volts
EXPANSION I/O				
OUTPUT VOLTAGE LOW		----	.4V	8 mA sink
OUTPUT VOLTAGE HIGH		2.4V	----	8 mA source
ENVIRONMENTAL				
TEMPERATURE -C VERSION		0ºC	70ºC	

REFERENCE INFORMATION

DRAWINGS