7I90HD EPP/SPI/SERIAL ANYTHING I/O MANUAL

Version 1.7

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GENERAL

DESCRIPTION

The MESA 7I90HD is a very low cost, general purpose, FPGA based programmable I/O card with a EPP parallel, RS-422 serial or SPI host interface.

Dual FPGA configuration EEPROMs allow simple recovery from programming mistakes. Firmware modules are provided for hardware step generation, quadrature encoder counting, PWM generation, digital I/O, Smart Serial remote I/O, BISS, SSI, SPI, UART interfaces and more.

All motion control firmware is open source and easily modified to support new functions or different mixes of functions.

All I/O bits are 5V tolerant and can sink 24 mA. All I/O pins support 3.3V LVDS signaling. Socketed pullup resistors are provided for all pins so that they may be connected directly to opto-isolators, contacts etc.

The 7I90HD has 72 I/O bits available on three 50 pin connectors, all connectors use I/O module rack compatible pinouts and are compatible with all Mesa 50 pin FPGA daughtercards.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I90HD card is oriented in an upright position, that is, with the EPP/SPI connector pointing towards the left.

CONNECTOR POWER

The 7I90HD has the option to supply 5V or 3.3V power from 7I90HDs I/O connectors to daughtercards.

The power option is individually selectable for each of the three I/O connectors. The 5V power is protected by per connector PTC devices so will not cause damage to the 7I90HD or system if accidentally shorted. The daughtercard voltage also selects the pullup resistor supply voltage for each connector. Note that all current Mesa daughtercards use 5V.

JUMPER	POS	FUNCTION
W6	UP	5V DAUGHTERCARD AND PULLUP POWER
W6	DOWN	3.3V DAUGHTERCARD AND PULLUP POWER

5V I/O TOLERANCE

The FPGA used on the 7I90HD has a 4V absolute maximum input voltage specification. To allow interfacing with 5V inputs, the 7I90HD has bus switches on all I/O pins. The bus switches work by turning off when the input voltage exceeds a preset threshold. *The 5V I/O tolerance option is the default and should normally be left enabled.*

For high speed applications where only 3.3V maximum signals are present and overshoot clamping is desired, the 5V I/O tolerance option can be disabled. W1 controls the 5V I/O tolerance option. When W1 is on the default UP position, 5V tolerance mode is enabled. When W1 is in the DOWN position, 5V tolerance mode is disabled. Note that W1 controls 5V tolerance on all I/O connectors.

HARDWARE CONFIGURATION

FPGA FLASH SELECT

To make recovery from FPGA configuration errors easier, there are two FPGA configuration flash memories on the 7I90HD card. Jumper W3 selects between the two flash memories. That is, if one flash memory is inadvertently corrupted, the other one can be used to boot the 7I90HD, allowing the corrupted flash memory to be re-written. It is suggested that W3 be left in the UP position (primary flash memory) for normal operation, and only changed to the DOWN position (secondary flash memory) if configuration fails. Once rebooted via a power cycle, jumper W3 should be promptly restored to the UP position to allow the primary flash memory to be re-written.

W3	**MEMORY**
UP	PRIMARY (NORMAL OPERATION)
DOWN	SECONDARY (BACKUP)

SECONDARY FLASH WRITE ENABLE

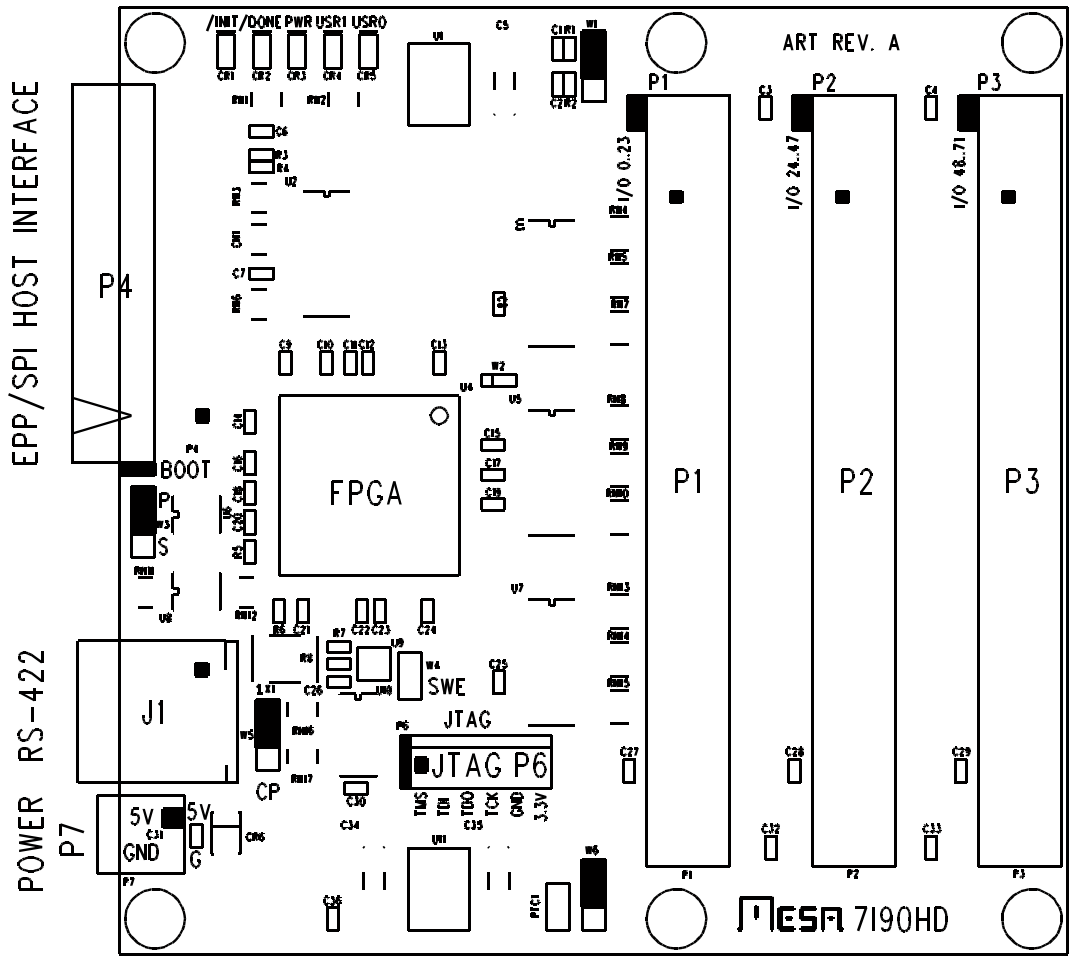
To prevent accidentally overwriting the secondary FPGA configuration, a jumper must be installed on jumper block W4 to enable writing to the secondary flash chip. When W4 is not present, the secondary flash is read-only.

RS-422 CABLE POWER

The 7I90HD can supply or source 5V power from its RS-422 connector J1 if desired. If cable power is selected, the 7I90 can be powered via a CAT5 interface cable. Cable power is compatible with Mesa serial daughtercards. W5 controls the cable power option. When W5 is in the up position, 5V power can be sourced or supplied by J1 pins 7 and 8. When W5 is in the down position, J1 pins 7 and 8 are unconnected.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

I/O CONNECTORS

The 7I90HD has 3 I/O connectors, P1 through P3. 7I90HD IO connector pinouts are as follows:

P1 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO0	2	GND	3	IO1	4	GND
5	IO2	6	GND	7	IO3	8	GND
9	IO4	10	GND	11	IO5	12	GND
13	IO6	14	GND	15	IO7	16	GND
17	IO8	18	GND	19	IO9	20	GND
21	IO10	22	GND	23	IO11	24	GND
25	IO12	26	GND	27	IO13	28	GND
29	IO14	30	GND	31	IO15	32	GND
33	IO16	34	GND	35	IO17	36	GND
37	IO18	38	GND	39	IO19	40	GND
41	IO20	42	GND	43	IO21	44	GND
45	IO22	46	GND	47	IO23	48	GND
49	POWER	50	GND				

CONNECTORS

I/O CONNECTORS

P2 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO24	2	GND	3	IO25	4	GND
5	IO26	6	GND	7	IO27	8	GND
9	IO28	10	GND	11	IO29	12	GND
13	IO30	14	GND	15	IO31	16	GND
17	IO32	18	GND	19	IO33	20	GND
21	IO34	22	GND	23	IO35	24	GND
25	IO36	26	GND	27	IO37	28	GND
29	IO38	30	GND	31	IO39	32	GND
33	IO40	34	GND	35	IO41	36	GND
37	IO42	38	GND	39	IO43	40	GND
41	IO44	42	GND	43	IO45	44	GND
45	IO46	46	GND	47	IO47	48	GND
49	POWER	50	GND				

CONNECTORS

I/O CONNECTORS

P3 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO48	2	GND	3	IO49	4	GND
5	IO50	6	GND	7	IO51	8	GND
9	IO52	10	GND	11	IO53	12	GND
13	IO54	14	GND	15	IO55	16	GND
17	IO56	18	GND	19	IO57	20	GND
21	IO58	22	GND	23	IO59	24	GND
25	IO60	26	GND	27	IO61	28	GND
29	IO62	30	GND	31	IO63	32	GND
33	IO64	34	GND	35	IO65	36	GND
37	IO66	38	GND	39	IO67	40	GND
41	IO68	42	GND	43	IO69	44	GND
45	IO70	46	GND	47	IO71	48	GND
49	POWER	50	GND				

CONNECTORS

POWER CONNECTOR PINOUT

P7 is the 7I90HDs power connector. P7 is a 3.5MM plug-in screw terminal block. P7 pinout is as follows:

PIN	FUNCTION	
1	+5V	TOP, SQUARE PAD
2	GND	BOTTOM, ROUND PAD

JTAG CONNECTOR PINOUT

P6 is a JTAG programming connector. This is normally used only for debugging or if both EEPROM configurations have been corrupted. In case of corrupted EEPROM contents the EEPROM can be re-programmed using Xilinx's Impact tool.

P6 JTAG CONNECTOR PINOUT

PIN	FUNCTION
1	TMS
2	TDI
3	TDO
4	TCK
5	GND
6	+3.3V

CONNECTORS

EPP/SPI CONNECTOR

P4 is the EPP printer port / SPI host interface connector. P4 is a 26 pin header. P4's pin-out matches stands DB25 printer port pin-out, allowing a simple flat cable with a DB25M IDC connector on one end and a 26 pin female header on the other end to interface the hosts printer port to the 7I90HD.

P4 PIN	DB25 PIN	SIGNAL	P4 PIN	DB25 PIN	SIGNAL
1	1	/STROBE	2	14	/AUTOFD
3	2	PD0	4	15	/FAULT
5	3	PD1	6	16	/INIT
7	4	PD2	8	17	/SELECTIN
9	5	PD3	10	18	GND
11	6	PD4 - SPICLK	12	19	GND
13	7	PD5 - SPIIN	14	20	GND
15	8	PD6 - SPIOUT	16	21	GND
17	9	PD7 - /SPICS	18	22	GND
19	10	/ACK	20	23	GND
21	11	BUSY	22	24	GND
23	12	PERROR	24	25	GND
25	13	SELECT	26	VCC	

CONNECTORS

RS-422 CONNECTOR

J1 is the 7I90HDs RS-422 serial interface. J1 is a RJ-45 jack. The serial interface pinout is compatible with standard 8 wire CAT5 Ethernet cables. J1 pinout is as follows:

PIN	SIGNAL	DIR	EIA/TIA 568B COLOR	
1	RXA	TO 7I90HD	ORANGE WHITE	
2	RXB	TO 7I90HD	ORANGE	
3	TXA	FROM 7I90HD	GREEN WHITE	
4	GND	EITHER	BLUE	
5	GND	EITHER	BLUE WHITE	
6	TXB	FROM 7I90HD	GREEN	
7	+5V	EITHER	BROWN WHITE	(5V if W5 is up)
8	+5V	EITHER	BROWN	(5V if W5 is up)

J1s pinout is designed to match breakout cards like the 7I44 and 7I74. A standard CAT5 or CAT5E cable can be used to connect the 7I90HD to a 7I44/7I74. CAT5E cable is suggested if the serial cable is used for powering the 7I90HD, as the larger wire size result in lower voltage drop.

OPERATION

FPGA

The 7I90HD use a Xilinx Spartan6 FPGA in a 144 pin TQFP package: XC6SLX9-TQG144.

HOST COMMUNICATION

Currenty there are four different host communication options available with standard 7I90HD firmware: EPP parallel and SPI (on P4) a LBP sserial slave and LBP16 remote HostMot2 using the RS-422 interface. EPP,SPI, and LBP16 can be used as host interfaces to the HostMot2 suite of I/O firmware, while the LBP implementation is used for a simple fixed purpose Smart Serial 72 bit I/O device.

EPP

The 7I90HDs EPP interface allows the 7I90HD to interface to PC parallel ports giving a medium speed real time interface (~1 Mbyte/sec) suited to motion control applications like LinuxCNC.

SPI

The 7I90HD SPI interface is also a medium speed real time (~1 to 5 Mbytes/sec) interface that allows simple interfacing to microcontrollers and SOCs.

LBP

LBP is a simple binary serial master slave protocol. The LBP implementation in the 7I90HD allows the 7I90HD to be use as a simple 72 I/O Smart Serial slave for remote TTL level interfacing.

LBP16

LBP16 is a simple binary serial master slave protocol suited to larger data blocks than LBP. LBP16 allows very large I/O expansion capabilities while maintaining a simple real time interface.

LBP HOST INTERFACE

The 7I90 can implement a simple remote sserial interface using LBP. This interface provides 72 I/O bits and is appropriate for applications like OPTO22 module rack I/O. The bit file for this mode is 7i90_ssremote.bit. For compatibility with I/O module racks, all I/O is open drain and active low. This allows any IO pin to be used as an input or output. Active low means a true input or output bit at the host is low at the 7I90 I/O pins. Pins that are used as inputs must have their corresponding outputs in the false state. In addition to the 72 GPIO bits, Three quadrature MPG counters are implemented on GPIO bits 48 through 53: 48=A0,49=B0,50=A1,51=B1,52=A2,53=B2.

A 50 ms watchdog timer is implemented and will set all outputs to a high state (via I/O pullups) if valid communications are not received at faster than a 50 ms/packet rate.

OPERATION

EPP HOST INTERFACE

The EPP host interface option allows the 7I90HD to connect to EPP compatible parallel port on PCs for a medium speed real time interface. The interface from host EPP printer port to the FPGA uses 12 FPGA pins. These consist of an eight bit bidirectional data bus (D0..D7), and four handshake lines.

P4 PIN	EPPNAME	SPPNAME	FPGA PIN	DIRECTION
1	/WRITE	/STROBE	40	TO FPGA
2	/DSTROBE	/AUTOFD	41	TO FPGA
8	/ASTROBE	/SELECTIN	48	TO FPGA
21	WAIT	BUSY	61	FROM FPGA
3	D0	D0	43	BIDIR
5	D1	D1	45	BIDIR
7	D2	D2	47	BIDIR
9	D3	D3	51	BIDIR
11	D4	D4	55	BIDIR
13	D5	D5	56	BIDIR
15	D6	D6	57	BIDIR
17	D7	D7	58	BIDIR

With standard HostMot2 EPP configurations, minumum AStrobe and Dstrobe durations are 200 nS. Read data is available in less than 70 nS from the strobe. Write data is sampled by the 7I90 180 nS from the beginning of the strobe, and wait is deasserted 200 nS from the beginning of the strobe.

OPERATION

SPI HOST INTERFACE

GENERAL

The SPI host interface is a medium speed real time host interface with a low pin count for microcontrollers and SOC's that have built in SPI interface hardware. The 7I90HDs SPI interface is a slave interface and uses a SPI frame size of 32 bits for all transactions. The interface supports a SPI clock rate up to 50 MHz.

SPI MODE

The host interface uses the convention that the clock idles low, host data is shifted into the 7I90HD on the SPI clock rising edge, and data is shifted out of the 7I90HD on the clock falling edge. This matches SPI master setup with CPOL=0 and CPHA=0. The CS pin is active low. To support the highest transfer rates the master should have a "late sample" option.

SPI HEADER

SPI transactions always starts with a 32 bit header which contains the target register address, the read or write command, the number of data elements to be transferred and the address increment bit.

SPI HEADER

A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	C	C	C	C	I	N	N	N	N	N	N	N	X	X	X	X

The first 16 bits ("A" in the table above) are the HostMot2 register address (byte address), MSb first. The next 4 bits ("C") are the command. Currently only 2 commands are supported, read (0xA) and write (0xB). The next bit ("I") is the address increment bit. When this bit is set, the register address is incremented (by 4) after every register read/write access, allowing burst transfers from groups of sequential registers without requiring a new address to be sent. Burst transfers with the increment bit cleared can be used for multiple reads/writes to a single address for FIFO access and similar applications. The next 7 bits ("N") are the burst length for sequential transfers.Valid burst lengths are 1 through 127. The "X" bits are unused.

TRANSFER SEQUENCE

For SPI reads the master sends the header followed by N frames of 32 dummy (0) bits, N being the burst length specified in the SPI header. The read data is returned on each 32 bit frame after the header frame.

On writes, the N frames of write data are sent by the master following the SPI header. The 7I90HD returns dummy data when write data is being received.

OPERATION

SPI HOST INTERFACE

DATA TRANSFER SEQUENCE

Example 1: Read 3 doublewords starting at 0x1000 with increment.

Master asserts /CS	
Master sends 0x1000A830	7I90HD echos dummy data
Master sends 0x00000000	7I90HD echos register data @0x1000
Master sends 0x00000000	7I90HD echos register data @0x1004
Master sends 0x00000000	7I90HD echos register data @0x1008
Master de-asserts /CS	

Example 2: Write 4 doublewords (A,B,C,D) to location 0x600C:

Master asserts /CS	
Master sends 0x600CB040	7I90HD echos dummy data
Master sends 0x0000000A	7I90HD echos dummy data
Master sends 0x0000000B	7I90HD echos dummy data
Master sends 0x0000000C	7I90HD echos dummy data
Master sends 0x0000000D	7I90HD echos dummy data
Master de-asserts /CS	

The master may de-assert /CS between frames or leave it asserted without affecting the SPI interface behavior as long as the CS idle time does not exceed the burst timeout value.

BURST TIMEOUT

Because the 7I90HD's SPI interface supports burst transfers of programmable length, its possible that an aborted or incorrect command could leave the 7I90HD in an unknown state. To recover from this condition, the 7I90HDs SPI interface has a timeout on bursts. The default timeout is 50 uSec. If /CS is de-asserted for 50 usec, the SPI interface will be reset (and any pending burst aborted) so that it expects a SPI header (a new command) as the next frame. A side effect of this timeout is that a burst transfer must never de-assert /CS for longer than 50 uSec during a burst.

SPI SIGNAL INTEGRITY

When using the SPI interface, signal quality is of very high importance. For best signal quality you should always use a flatcable with all 8 ground wires on P4 connected to the SPI master. In addition, the SPI master clock signal should be series terminated so that it has a 130 Ohm total source resistance to match the flat cable impedance. This typically means adding a ~47 Ohm series resistor in the SPI CLK line at the master end.

OPERATION

LBP16 HOST INTERFACE

GENERAL

The LBP16 serial host interface is a high speed (to 10 Mbits/sec) RS-422 host interface suited to remote data acquisition and distributed I/O systems. Like the other host interfaces the LBP16 allows all of the standard HostMot2 I/O modules to be used. LBP16 uses standard asynchronous communication.

CONNECTIONS

The RJ45 connector J1 is used for LBP16 serial communications. This connector matches the pinout of MESAs 7I74 and 7I44 daughtercards for FPGA host interfaces, so only a standard CAT5 cable is needed.

SETUP OPTIONS

The current LBP16 firmware has no EEPROM setup options but has 2 jumper selectable options, Low_Baud and CRC_Disable. These options are intended to simplify testing and allow 115200 baud rate for firmware updating via normal USB-serial adapters. These options are selected by grounding pins on the EPP/SPI interface connector. This can be accomplished easily by installing standard .1" shunts across pins on P4 since the even numbered pins are grounded and the signal pins have pullup resistors.

	HIGH (OPEN)	LOW (SHORTED)
P4 pins 23,24	2.5 M Baud	115.2 K Baud
P4 pins 21,22	CRC enabled	CRC disabled

Note that setting the low baud rate option sets the packet framing timeout to 25 character times instead of the normal 2 character times. This is to make access easier with standard serial ports and USB/serial adapters.

PROTOCOL

For detailed information on the LBP16 serial protocol, see the reference section of this manual

OPERATION

PC HOST ADAPTER

In order to run any of the serial command line utilities a RS-422 adapter is needed. Mesa can provide a suitable adapter. Two such adapters are 3I21 or 3I22. These adapters connects the RJ-45 RS-422 interface on the 7I90HD to a DB9 serial port (3I21) or USB port (3I22) and provide 5V link power.

MINIMAL HOST PC ADAPTER

A simple home made host adapter can be made by directly connecting RS-232 signals from a 9 pin PC serial port or USB RS-232 adapter to the 7I90HD's RS-422 signals via a one ended CAT5 cable. A single resistor between RS-232 TXD and RS-422 RXB is needed to prevent overloading the RS-232 TXD output

CAT5 PIN	DE-9F PIN	CAT5 SIGNAL	DE-9F SIGNAL	CAT5 COLOR
1	5	RXA	GND	ORANGE WHITE
2	3	RXB (1)	TXD (1)	ORANGE
3	XX	TXA	XX	GREEN WHITE
4	5	GND	GND	BLUE
5	5	GND	GND	BLUE WHITE
6	2	TXB	RXD	GREEN
7	XX	+5V (2)	XX	BROWN WHITE
8	XX	+5V (2)	XX	BROWN

Notes:

1. Connect via 470 Ohm 1/4 watt resistor. All other signals directly connected

2. If not supplied by the adapter, +5V power must be supplied via the 7I90HDs 5V power connector P7

OPERATION

CONFIGURATION

The 7I90HD is configured at power up by a SPI FLASH memory. This flash memory is an 8M bit chip that has space for two configuration files. Since all host interface logic on the 7I90HD is in the FPGA, a problem with configuration means that host access will not be possible. For this reason there are two backup methods to recover from FPGA boot failures.

FALLBACK

The first backup system is called Fallback. The7I90HD flash memory normally contains two configuration file images, A user image and a fallback image. If the primary user configuration is corrupted, the FPGA will load the fallback configuration so the flash memory image can be repaired remotely without having to resort to switching memories or JTAG programming.

DUAL EEPROMS

The second backup method relies on the fact that there are two flash memories on the 7I90HD card, selectable via jumper W3. If a configuration fails in such a way that it loads correctly (has a valid CRC) but does not work, the fallback configuration will not be invoked. To recover from this problem, the secondary flash can be selected by moving W3 to the DOWN position and using it to boot the FPGA (by cycling the power), restoring remote access and allowing the primary configuration to be repaired via the host interface.

The backup EEPROM is write protected tp prevent accidental overwriting the secondary (backup) configuration. If the primary EEPROM has been corrupted, you can boot from the secondary configuration, but you must restore W3 to the UP position to allow re-writing the primary configuration. If the secondary configuration needs to be re-written, W4 must be installed to allow writes. Once the secondary EEPROM is written, W4 should be removed.

OPERATION

EEPROM LAYOUT

The EEPROMs used on the 7I90HD for configuration storage are Micron M25P80's. The M25P80 is a 8 M bit (1 M byte) EEPROM with sixteen 64K byte sectors. Configuration files are stored on sector boundaries to allow individual configuration file erasing and updating. Standard EEPROM sector layout is as follows:

0x000000	**BOOT BLOCK**
0x010000	**FALLBACK CONFIGURATION BLOCK 0**
0x020000	**FALLBACK CONFIGURATION BLOCK 1**
0x030000	**FALLBACK CONFIGURATION BLOCK 2**
0x040000	**FALLBACK CONFIGURATION BLOCK 3**
0x050000	**FALLBACK CONFIGURATION BLOCK 4**
0x060000	**FALLBACK CONFIGURATION BLOCK 5**
0x070000	**RESERVED**
0x080000	**USER CONFIGURATION BLOCK 0**
0x090000	**USER CONFIGURATION BLOCK 1**
0x0A0000	**USER CONFIGURATION BLOCK 2**
0x0B0000	**USER CONFIGURATION BLOCK 3**
0x0C0000	**USER CONFIGURATION BLOCK 4**
0x0D0000	**USER CONFIGURATION BLOCK 5**
0x0E0000	**UNUSED/FREE**
0x0F0000	**UNUSED/FREE**

OPERATION

BITFILE FORMAT

The configuration utilities expects standard FPGA bitfiles without any multiboot features enabled. If multiboot FPGA files are loaded they will likely cause a configuration failure. In addition for fallback to work, the -g next_config_register_write:disable, -g reset_on_error:enable and -g CRC:enable bitgen options must be set.

MESAFLASH

Linux and Windows utility programs mesaflash and mesaflash.exe are provided to write configuration files to the 7I90HD EEPROM via the RS-422 interface and LBP16. The linux utility can also write configuration files via the EPP interface. These files depend on a simple SPI interface built into both the standard user FPGA bitfiles and the fallback bitfile.

If mesaflash is run with no command line arguments it will print usage information

mesaflash --device 7I90 --port 0x378 --write FPGAFILE.BIT.

Writes a standard bitfile FPGAFILE.BIT to the user area of the EEPROM

mesaflash --device 7I90 --port 0x378 --verify FPGAFILE.BIT

Verifies the user EEPROM configuration against the bit file FPGAFILE.BIT.

mesaflash --device 7I90 --port 0x378 --fallback --write fallback.bit

Writes the fallback EEPROM configuration to the fallback area of the EEPROM. In addition if the bootblock is not present in block 0 of the EEPROM, it re-writes the bootblock.

OPERATION

FREE FLASH MEMORY SPACE

Two 64K byte blocks of flash memory space are free when both user and fallback configurations are installed on the 7I90HD.

FALLBACK INDICATION

Mesa's supplied fallback configurations blink the red INIT LED on the top right hand side of the card if the primary configuration fails and the fallback configuration loaded successfully. If this happens it means the user configuration is corrupted or not a proper configuration for the 7I90HDs FPGA. This can be fixed by running the configuration utility and re-writing the user configuration**.**

FAILURE TO CONFIGURE

The 7I90HD should configure its FPGA within a fraction of a second of power application. If the FPGA card fails to configure, the red /DONE LED CR2 will remain illuminated. If this happens the secondary EEPROM boot should be used. If booting from the secondary EEPROM fails, the 7I90HDs EEPROMs must be re-programmed via the JTAG connector or (faster) JTAG FPGA load followed by EPP or LBP16 EEPROM update.

CLOCK SIGNALS

The 7I90HD has a single 50 MHz clock signal from an on card crystal oscillator. The clock a can be multiplied and divided by the FPGAs clock generator block to generate a wide range of internal clock signals.

OPERATION

LEDS

The 7I90HD has two FPGA driven user LEDs (User 0 and User 1 = Green), and three status LEDs (two red and one yellow). The user LEDs can be used for any purpose, and can be helpful as a simple debugging feature. A low output signal from the FPGA lights the LED. See the 7I90HDIO.PIN file for FPGA pin locations of the LED signals. The status LEDs reflect the state of the FPGA's /INIT, DONE pins and 3.3V power. The /DONE LED lights until the FPGA is configured at power-up. The /INIT LED lights when the power on reset is asserted, when there has been a CRC error during configuration. The yellow PWR leds lights when 3.3V power is present on card. When using Mesas configurations, the /INIT LED blinks when the fallback configuration has been loaded.

PULLUP RESISTORS

All I/O pins are provided with pull-up resistors to allow connection to open drain, open collector, or OPTO devices. These resistors have a value of 3.3K so have a maximum pull-up current of ~1.07 mA (5V pull-up) or ~.7 mA (3.3V pull-up).

IO LEVELS

The Xilinx FPGAs used on the 7I90HD have programmable I/O levels for interfacing with different logic families. The 7I90HD does not support use of the I/O standards that require input reference voltages. All standard Mesa configurations use LVTTL levels.

Note that even though the 7I90HD can tolerate 5V signal inputs in 5V tolerance mode, its outputs will not swing to 5V. The outputs are push pull CMOS that will drive to the output supply rail of 3.3V. This is sufficient for TTL compatibility but may cause problems with some types of loads. For example when driving an LED that has its anode connected to 5V, in such devices as OPTO isolators and I/O module rack SSRs, the 3.3V high level may not completely turn the LED off. To avoid this problem, either drive loads that are ground referred, use 3.3V as the VCC for VCC referred load or use open drain mode in conjunction with 5V tolerance mode. When this is done, the outputs will be pulled up to 5V when off**.**

STARTUP I/O VOLTAGE

After power-up or system reset and before the the FPGA is configured, the pull-up resistors will pull all I/O signals to a high level. If the FPGA is used for motion control or controlling devices that could present a hazard when enabled, external circuitry should be designed so that this initial state (high) results in a safe condition.

SUPPLIED CONFIGURATIONS

HOSTMOT2

All supplied configurations are part of the HostMot2 motion control firmware set. All HostMot2 firmware is open source and easily extendible to support new interfaces or different sets of interfaces embedded in one configuration. For detailed register level information on Hostmot2 firmware modules, see the regmap file in the hostmot2 source code directory. Note that all configurations are available with EPP, SPI or LBP16 serial host interfaces.

SVST8_4IM2

SVST8_4IM2 is a 8 axis servo/ 4 axis stepmotor configuration with 8 PWM outputs, 8 encoder inputs with index mask, 4 hardware stepgenerators, a watchdog timer and GPIO.

SVST4_8

SVST4_8 is a 4 axis servo/ 8 axis stepmotor configuration with 4 PWM outputs, 4 encoder inputs, 8 hardware stepgenerators, a watchdog timer and GPIO.

SVST8_8IM2

SVST8_8IM2 is a 8 axis servo/ 8 axis stepmotor configuration with 8 PWM outputs, 8 encoder inputs with index mask, 8 hardware stepgenerators, a watchdog timer and GPIO.

SVST1_4_7I47S

SVST1_4_7I47S is a 4 axis stepmotor configuration with 1 PWM output for spindle, and 4 encoder inputs, a watchdog timer and GPIO. For the 7I47S card.

2X7I65

2X7I65 is a configuration for up to two 7I65 octal analog servo interface cards. It has 16 encoder inputs, 2 SPI ports, a watchdog timer and GPIO.

SV12IM_2X7I48

SV12IM_7I48 is a 12 axis servo configuration fro two 7I48 daughter cards. It has 12 encoder inputs, 12 PWM outputs, a watchdog timer and GPIO.

SV6_7I49

SV6_7I49 is a six axis servo configuration for use with the 7I49 resolver input daughter card. Its has a 6 channel resolver interface, 6 pwm channels, a watchdog timer and GPIO.

SUPPLIED CONFIGURATIONS

PIN FILES

Each of the configurations has an associated file with file name extension .pin that describes the FPGA functions included in the configuration and the I/O pinout. These are plain text files that can be printed or viewed with any text editor.

REFERENCE INFORMATION

LBP16

LBP16 COMMANDS

LBP16 is a simple remote register access protocol to allow efficient register access over a serial link. All LBP16 commands are 16 bits in length and have the following structure:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	A	C	M	M	M	S	S	I	N	N	N	N	N	N	N

W Is the write bit (1 means write, 0 means read)

A Is the includes Address bit. If this is '1' the command is followed by a 16 bit address and the address pointer is loaded with this address. if this is 0 the current address pointer for the memory space is used. Each memory space has its own address pointer.

C Indicates if memory space itself (C=’0') or associated info area for the memory will be accessed (C= ‘1')

M Is the 3 bit memory space specifier 000b through 111b

S Is the transfer element size specifier (00b = 8 bits, 01b = 16 bits 10b = 32 bits and 11b = 64 bits)

I Is the Increment address bit. if this is '1' the address pointer is incremented by the element transfer size (in bytes) after every transfer ('0' is useful for FIFO transfers)

N Is the transfer count in units of the selected size. 1 through 127. A transfer count of 0 is an error.

LBP16 read commands are followed by the 16 bit address (if the A bit is set). LBP16 Write commands are followed by the address (if bit A is set) and the data to be written. LBP16 Addresses are always byte addresses. LBP data and addresses are little endian so must be sent LSB first.

REFERENCE INFORMATION

LBP16

CRC

If CRCs are enabled all transmitted and received messages have a 16 bit CRC appended to the message. The CRC polynomial is X^16 +X^12 +X^5 +1 (CRC-CCITT) The varient used is CRC-CCITT-KERMIT.

FRAMING

Packet framing in accomplished with timed gaps in transmitted data. Default packet frame timeout is 2 character times at high baud rates and 25 character times at 115200 baud.

REFERENCE INFORMATION

LBP16

INFO AREA

There are eight possible memory spaces in LBP16. Each memory space has an associated read only info area. The first entry has a cookie to verify correct access. The next two entries in the info area are the MemSizes word and the MemRanges word. Only 16 bit read access is allowed to the info area.

0000	COOKIE = 0X5A0N WHERE N = ADDRESS SPACE 0..7
0002	MEMSIZES
0004	MEMRANGES
0006	ADDRESS POINTER
0008	SPACENAME 0,1
000A	SPACENAME 2,3
000C	SPACENAME 4,5
000E	SPACENAME 6,7

INFO AREA MEMSIZES FORMAT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	T	T	T	T	T	T	T	X	X	X	X	A	A	A	A

W Memory space is Writeable

T Is type: 01 = Register, 02 = Memory, 0E = EEPROM, 0F = Flash

A Is access types (bit 0 = 8 bit, bit 1 = 16 bit etc)so for example 0x06 means 16 bit and 32 bit operations allowed

REFERENCE INFORMATION

LBP16

INFO AREA MEMRANGES FORMAT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E	E	E	E	E	P	P	P	P	P	S	S	S	S	S	S

E Is erase block size

P Is Page size

S Ps address range

Ranges are 2^E, 2^P, 2^S. E and P are 0 for non-flash memory

REFERENCE INFORMATION

LBP16

INFO_AREA ACCESS

As discussed above, all memory spaces have an associated information area that describes the memory space. Information area data is all 16 bits and read-only.The hex command examples below are written in LSB first order for convenience. In the hex command examples, the NN is the count/increment field of the LBP16 command and the LLHH is the low and high bytes of the address.

Ispace 0 read with address	NN61LLHH	HostMot2 space
Ispace 0 read	NN21	
Ispace 1 read with address	NN65LLHH	Unused
Ispace 1 read	NN25	
Ispace 2 read with address	NN69LLHH	Unused
Ispace 2 read	NN29	
Ispace 3 read with address	NN6DLLHH	FPGA flash space
Ispace 3 read	NN2D	
Ispace 4 read with address	NN71LLHH	Timer/Utility space
Ispace 4 read	NN21	
Ispace 5 read with address	NN75LLHH	Unused
Ispace 5 read	NN75	
Ispace 6 read with address	NN79LLHH	LBP16 R/W space
Ispace 6 read	NN39	
Ispace 7 read with address	NN7DLLHH	LBP16 R/O space
Ispace 7 read	NN3D	

REFERENCE INFORMATION

LBP16

7I90HD SUPPORTED MEMORY SPACES

The 7I90HD firmware supports 7 address spaces. These will be described individually with example hexadecimal commands. The hex command examples below are written in LSB first order for convenienc5901e. In the hex command examples, the NN is the count/increment field of the LBP16 command and the LLHH is the low and high bytes of the address.

SPACE 0: HOSTMOT2 REGISTERS

This address space is the most important as it gives access to the FPGA I/O. This is a 64K byte address range space with 32 bit R/W access.

Space 0 read with address	NN42LLHH
Space 0 write with address	NNC2LLHH
Space 0 read	NN02
Space 0 write	NN82

REFERENCE INFORMATION

LBP16

SPACE 0: HOSTMOT2 REGISTERS

Example: read first 5 entries in hostmot2 IDROM:

85420004

85 ; 85 == NN = 5 | Inc bit (0x80) so address is incremented after each access

42 ; Read from space 0 with address included after command

00 ; LSB of address (IDROM starts at 0x0400)

04 ; MSB of address (IDROM starts at 0x0400)

Example: write 3 GPIO ports starting at 0x1000:

83C20010AAAAAAAABBBBBBBBCCCCCCCC

83 ; 83 == NN = 3 | Inc bit so address is incremented after each access

C2 ; Write to space 0 with address included after command

00 ; LSB of address (GPIO starts at 0x1000)

10 ; MSB of address (GPIO starts at 0x1000)

AAAAAAAA ; 32 bit data for GPIO port 0 at 0x1000

BBBBBBBB ; 32 bit data for GPIO port 0 at 0x1004

CCCCCCCC ; 32 bit data for GPIO port 0 at 0x1008

Note: like all LBP16 data, write data is LS byte first.

REFERENCE INFORMATION

LBP16

SPACE 3: FPGA FLASH EEPROM CHIP ACCESS

Space 3 allows access to the FPGAs configuration flash memory. All flash memory access is 32 bit. Flash memory access is different from other memory spaces in that it is done indirectly via a 32 bit address pointer and 32 bit data port.

Space 3 read with address NN4ELLHH

Space 3 write with address NNCELLHHDDDDDDDD

Space 3 read NN0E

Space 3 write NN8E

FLASH MEMORY REGISTERS

Flash memory spaces have only 4 accessible registers:

ADDRESS	DATA	
0000	FL_ADDR	32 bit flash address register
0004	FL_DATA	32 bit flash data register
0008	FL_ID	32 bit read only flash ID register
000C	SEC_ERASE	32 bit write only sector erase register

Unlike other memory spaces, flash memory space is accessed indirectly by writing the address register (FL_ADDR) and then reading or writing the data (FL_DATA). The flash byte address is automatically incremented by 4 each data access.

Note that reads can read all of flash memory with consecutive read operations but write operations can only write a flash page worth of data before the page write must be started. Also unless you are doing partial page writes, page write should always start on a page boundary.

The page write is started by writing the flash address, reading the flash address, reading flash data, reading flash ID or issuing a erase sector command. For host synchronization, a read operation should follow every sector erase or page write.

REFERENCE INFORMATION

LBP16

SPACE 3: FPGA FLASH EEPROM CHIP ACCESS

Example: read 1024 bytes (0100h doublewords) of flash space at address 00123456:

01CE000056341200	Write FL_ADDR (0000) with pointer (0x00123456)
404E0400	Issue read command (FL_DATA = 0004) With count of 0x40 double words (256 bytes). Note do not use LBP16 increment bit! Flash address always autoincremented
400E	Next 0x40 doublewords = 256 bytes
400E	Next 0x40 doublewords = 256 bytes
400E	Next 0x40 doublewords = 256 bytes

Note that this is close to the maximum reads allowed in a single LBP packet (~1450 bytes)

Writes and erases require that the EEPROMWEna be set to 5A03. *Note that EEPROMWEna is cleared at the end of every LPB packet so the write EEPROMWEna command needs to prepended to all flash write and erase packets. The following is written on separate lines for clarity but must all be in one packet for correct operation.*

Example: Write a 256 byte page of flash memory starting at 0xC000:

01D91A00035A	Write EEPROMWEna with 0x5A03
01CE000000C00000	Write flash address
40CE0400	Issue write flash data command with count
12345678	Doubleword 0
ABCD8888	Doubleword 1
...	
FFFFFFFF	Doubleword 63 (= 256 bytes)
014E0000	Read new address to commit write and so some data is returned for host synchronization (so host waits for write to complete)

REFERENCE INFORMATION

LBP16

SPACE 3: FPGA FLASH EEPROM CHIP ACCESS

Example: Erase flash sector 0x00010000:

01D91A00035A	Write EEPROMWEna with 0x5A03
01CE000000000100	Write flash address with 0x 00010000
01CE0C0000000000	Write sector erase command (with dummy 32 bit data = 0)
014E0000	Read flash address for host synchronization (this will echo the address _after_ the sector is erased)

REFERENCE INFORMATION

LBP16

SPACE 4 LBP TIMER/UTILITY AREA

Address space 4 is for read/write access to LBP specific timing registers. All memory space 4 access is 16 bit.

Space 4 read with address	NN51LLHH
Space 4 write with address	NND1LLHHDDDD
Space 4 read	NN11
Space 4 write	NN91DDDD

MEMORY SPACE 4 LAYOUT:

ADDRESS	DATA
0000	uSTimeStampReg
0002	WaituSReg
0004	HM2Timeout
0006	WaitForHM2RefTime
0008	WaitForHM2Timer1
000A	WaitForHM2Timer2
000C	WaitForHM2Timer3
000E	WaitForHM2Timer4

The uSTimeStamp register reads the free running hardware microsecond timer. It is useful for timing internal 7I90 operations. Writes to the uSTimeStamp register are a no-op. The WaituS register delays processing for the specified number of microseconds when written, (0 to 65535 uS) reads return the last wait time written. The HM2TimeOut register sets the timeout value for all WaitForHM2 times (0 to 65536 uS).

All the WaitForHM2Timer registers wait for the rising edge of the specified timer or reference output when read or written, write data is don't care, and reads return the wait time in uS. The HM2TimeOut register places an upper bound on how long the WaitForHM2 operations will wait. HM2Timeouts set the HM2TImeout error bit in the error register.

REFERENCE INFORMATION

LBP16

SPACE 6 LBP STATUS/CONTROL AREA

Address space 6 is for read/write access to LBP specific control, status, and error registers. All memory space 6 access is 16 bit. The RXUDPCount and TXUDPCount can be used as sequence numbers to verify packet reception and transmission.

Space 6 read with address	NN59LLHH
Space 6 write with address	NND9LLHHDDDD
Space 6 read	NN19
Space 6 write	NN99DDDD

MEMORY SPACE 6 LAYOUT:

ADDRESS	DATA
0000	ErrorReg
0002	LBPParseErrors
0004	LBPMemErrors
0006	LBPWriteErrors
0008	RXPktCount
000A	RXGoodCount
000C	RXBadCount
000E	TXPktCount
0010	TXGoodCount
0012	TXBadCount

REFERENCE INFORMATION

LBP16

MEMORY SPACE 6 LAYOUT:

ADDRESS	DATA	
0014	LEDMode	If LSb is 0, LEDs are "owned" by HostMot2, otherwise LEDs are local debug LEDs
0016	DebugLEDPtr	What variable in space 6 local debug LEDs show (default is RXPktCount).
0018	Scratch	Can be used for sequence numbers
001A	EEPROMWEna	Must be set to 5A0N enable EEPROM or flash writes or erases (N is memory space of EEPROM or flash) Note that this is cleared at the end of every packet.
001C	LBPReset	Setting this to a non-zero value with do a full reset of the LBP16 firmware. The 7I90HD will be unresponsive for as much as ½ a second after this command.

ERROR REGISTER FORMAT

BIT	ERROR
0	LBPParseError
1	LBPMemError
2	LBPWriteError
3	RXPacketError
4	TXPacketError
5	HM2TimeOutError
6..15	Reserved

REFERENCE INFORMATION

LBP16

SPACE 7: LBP READ ONLY AREA

Memory space 7 is used for read only card information. Memory space 7 is accessed as 16 bit data.

Space 7 read with address	NN5DLLHH
Space 7 read	NN1D

MEMORY SPACE 7 LAYOUT:

ADDRESS	DATA	
0000	CardNameChar-0,1	
0002	CardNameChar-2,3	
0004	CardNameChar-4,5	
0006	CardNameChar-6,7	
0008	CardNameChar-8,9	
000A	CardNameChar-10,11	
000C	CardNameChar-12.13	
000E	CardNameChar-14,15	
0010	LBPVersion	
0012	FirmwareVersion	
0014	Option Jumpers	
0016	Reserved	
0018	RecvStartTS	1 uSec timestamps
001A	RecvDoneTS	For performance monitoring
001C	SendStartTS	Send timestamps are
001E	SendDoneTS	from ***previous*** packet

REFERENCE INFORMATION

SPECIFICATIONS

POWER	MIN	MAX	NOTES:
5V POWER SUPPLY	4.5V	5.5V	P4 supplied 5V
5V POWER CONSUMPTION:	----	3A	Depends on FPGA configuration and external load
INPUT VOLTAGE (3.3V mode)	-0.6V	4V	
INPUT VOLTAGE (5V mode)	-0.6V	7V	
VOL	----	0.5V	20 mA sink
VOH	----	2.8V	20 mA source (3.3V mode)
RS-422 DATA RATE	----	10 MBaud	
MAX 5V CURRENT TO I/O CONNS	---	400 mA	Each (PTC Limit)
TEMPERATURE RANGE -C version	0 ^{o}C	+70 ^{o}C	
TEMPERATURE RANGE -I version	-40 ^{o}C	+85 ^{o}C	

REFERENCE INFORMATION

CARD DRAWING