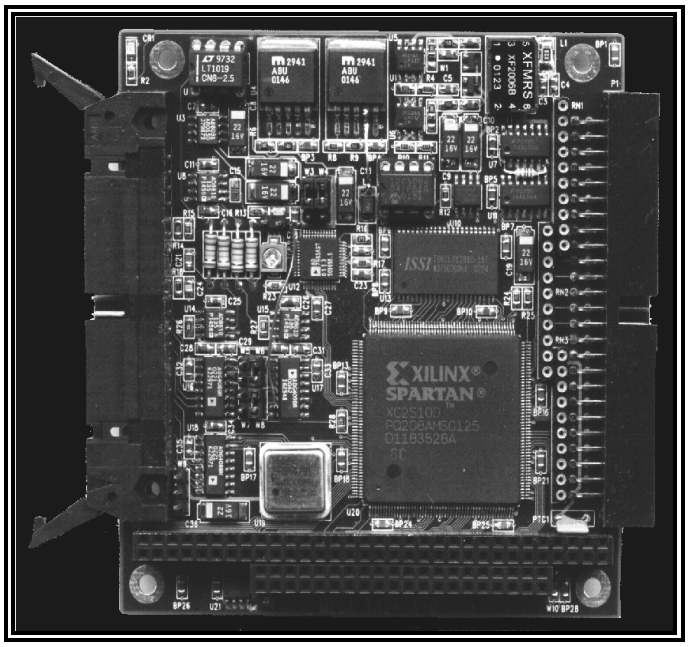
4A24 16 BIT 200/500KHz A-D

- **16 bit resolution**
- **+-5 and +-2.5V input ranges**
- **200 KHz or 500 KHz conversion rate**
- **16 single ended or 8 diff. Inputs**
- **128K sample FIFO buffer**
- **EEPROM calibration storage**
- **Polled or interrupt driven mode**
- **Autozero and signal averaging**
- **24 bits of general purpose I/O**
- **Made in USA - local support**
- **Single 5V power supply**
- **2 year warranty**



The 4A24 is a high resolution, high speed, low cost A-D card for the PC/104 bus. 200 Khz and 500 KHz models are available. On card EEPROM calibration storage and fully digital zero and span calibration eliminates potentiometers and simplifies circuitry.

A high bandwidth instrumentation amplifier is used for the input. Input channel scan sequence, averaging, option, raw/calibrated data choice, and autozero option are determined by a built-in 1024 entry function table. Four function table extended multiplexor select addresses are available from the I/O connector for submultiplexing or other functions.

The averaging option in the function table allows A-D data on selected channels to be averaged from 2 to 128 times for noise reduction.

Converted data is placed in a 128K word sample FIFO so that host latency requirements are relaxed.

Conversions can be started by the timer, an external start convert input, or the host processor. Timed burst conversions (1 to 2^32-1 conversions) can be started by the host or the external start convert input.

The conversion start timer is a 24 bit, 50 MHz programmable divider for high resolution and wide conversion rate range.

The 4A24 can operate in polled or interrupt driven mode. In polled mode, the data available status of the FIFO is read from a status port and if data as available, the FIFO port can be read. In the simplest polled mode, the host writes to the FIFO port to start a conversion, polls the status register for the DAV flag and then reads the A-D data from the FIFO port.

In interrupt driven mode, an interrupt is generated when the 128K word FIFO reaches a predetermined count. At this point the host can do a block I/O read from the FIFO to efficiently transfer the data to the host. The 4A24 can be programmed to use any of the available PC/104 bus interrupts.

24 general purpose I/O bits are provided. Each I/O bit can be individually programmed to be an input or output. Optional pullups are provided for all I/O bits.

All main digital logic on the 4A24 is contained in a FPGA to allow field upgradability and customization for special applications.

4A24 ANALOG CONNECTOR PINOUT:

PIN#	SIGNAL	PIN#	SIGNAL
1	SHIELD GND	21	SHIELD GND
2	SHIELD GND	22	SHIELD GND
3	AIN0	23	INPUT COMMON
4	AIN1	24	INPUT COMMON
5	AIN2	25	VREF (2.5V)
6	AIN3	26	VREF (2.5V
7	AIN4	27	INPUT GND
8	AIN5	28	INPUT GND
9	AIN6	29	SHIELD GND
10	AIN7	30	SHIELD GND
11	SHIELD GND	31	EXT START CONVERT
12	SHIELD GND	32	SHIELD GND
13	AIN8	33	MUXA3
14	AIN9	34	MUXA4
15	AIN10	35	MUXA5
16	AIN11	36	MUXA6
17	AIN12	37	MUXA7
18	AIN13	38	NC
19	AIN14	39	5V (PTC)
20	AIN15	40	SHIELD GND

ORDERING INFORMATION:

4A24	PC/104 16 BIT HIGH SPEED A-D CARD

Add -I for industrial temperature range.